AMENDMENTS TO THE SPECIFICATION

Following page 5, line 28, add the following two new paragraphs:

Figure 1C(1) illustrates a layout diagram of a prior art single port SRAM having overall dimensions of 1.3 um by 1.9 um for a cell size area of 2.47 um^2.

Figure 1C(2) illustrates a layout diagram of the present invention dual port SRAM having overall dimensions of 1.3 um by 2.3 um for a cell size area of 2.99 um^2.

On page 6, below the table and above line 4, add the following paragraph:

Fig. 2 illustrates an interleaved write operation for a dual port static(S) RAM having RAM-A and RAM-B, having row addresses, A1, A2, A3, A4, A5 and A6, datas D1, D2, D3, D4, D5 and D6, and executing interleaved write operations W1, W2, W3, W4, W5 and W6. In the interleaved write operations, the first data is written into the first array RAM-A in a first write operation W1, and after ½ cycle the second data is written into the second array RAM-B in a second write operation W2.

Page 6, following line 7, add the following new paragraph:

Fig. 3 illustrates an interleaved read operation for a dual port static(S) RAM, having RAM-A and RAM-B, wherein either the first port or second port can be used for row accessing. The dual port static(S) RAM has row addresses A1, A2, A3, A4, A5 and A6, and executes interleaved read operations R1, R2, R3, R4, R5 and R6 at different wordlines.

Amend the paragraph on page 7, lines 8-19, with the following replacement paragraph:

Each read operation can be through either port of the RAM. Therefore, within all ½ cycle, almost all wordlines in both arrays can be accessed for a read operation. During each read, since the bit-lines drop to almost 100 mV, a disturb due to two wordline activations

through different ports is not a concern. As shown in the example of Fig. 3, a first wordline ~~R1~~ is selected for a read R1 in RAM-A, and therefore either the first port or second port can be used for row accessing. After ½ cycle, a second wordline ~~R2~~ residing in RAM-B is activated for a read R2, so the first port is used for the row access. After the next ½ cycle, a third wordline in the same array RAM-B is accessed, and then the second port must be used for read R3'. Similarly, read R4 also occurs in the ½ cycle to the first port, while reads R5' and R6 are located in the same array RAM-A via two different ports. In summary, interleaved read or write operations can boost the cycle time to about 1 ns, so that the SRAM will appear to operate at 1GHz.